0.25μm pHEMT 40Gb/s E/O Modulator Drivers

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Abstract – **The development of two high voltage, 40 Gb/s E/O modulator driver ICs is described. Both were designed with a Distributed Amplifier (DA) topology utilizing a 0.25μm GaAs pHEMT production process. The modulator drivers exhibit 6dB of small signal gain, greater than 42 GHz of 3dB bandwidth, and better than 6.5-V_{PP} output swing.**

I. Introduction

Fiber systems have received much attention because of the immense opportunities they present to component manufacturers. Systems at 40 Gb/s speeds are aggressively being developed in order to offer lower cost per transmitted bit than the present 10 Gb/s systems. The 40 Gb/s system cost is critical and must remain less than 2.5 times a 10 Gb/s system's cost to be commercially attractive [1]. Most manufacturers of 40 Gb/s physical layer components have focused on wide bandwidth performance by using technologies with the highest F_τ available, which tend to be the least mature and most expensive solutions. Meanwhile, system designers are waiting for low cost components with just enough performance. Excellent 40 Gb/s results have been published demonstrating distributed amplifiers developed in various advanced technologies [2]. However, GaAs technology has largely been discounted as a practical approach to design into the 40 Gb/s market.

This work demonstrates that 0.25μm pHEMT is a viable technology choice because it offers the lowest cost solution for the required performance for many 40 Gb/s system components. In particular, wide bandwidth with high output drive voltages are key components features that can be addressed with a less exotic technology such as GaAs pHEMT [3]. This paper describes two amplifiers developed on TriQuint's production 0.25-μm GaAs pHEMT technology that are cost-effective circuits demonstrating 40 Gb/s performance.

II. E/O Modulator Design

The design goals for both driver ICs were 8dB of small signal gain and an output voltage in excess of 6.5-V_{PP} at a 40 Gb/s data rate. The high voltage swing supports modulators commonly used in the transmit section of fiber optic systems such as Lithium Niobate Mach-Zehnders. A 6.5-V_{PP} output voltage swing provides margin for system losses and modulator V_π variability.

The cascode device topologies illustrated in Figure 1 provide increased cell gain as well as high output impedance [4]. Cascode cells also allow for data eye level and crossing adjustment which increases circuit flexibility. Two different cell topologies were used in this effort to mitigate risk. The first cell pictured in Figure 1c was considered the least risky and was composed of separate common source and a common gate FET cells separated by a length of microstrip transmission line. The second approach used a dual gate cell configuration pictured in Figure 1d. The dual gate cell was constructed with separate FET gate channels separated by a short metal strip. It can be easily seen from the SEM photographs that the dual gate implementation is the smaller of the two and therefore has an inherent advantage from a total size perspective.

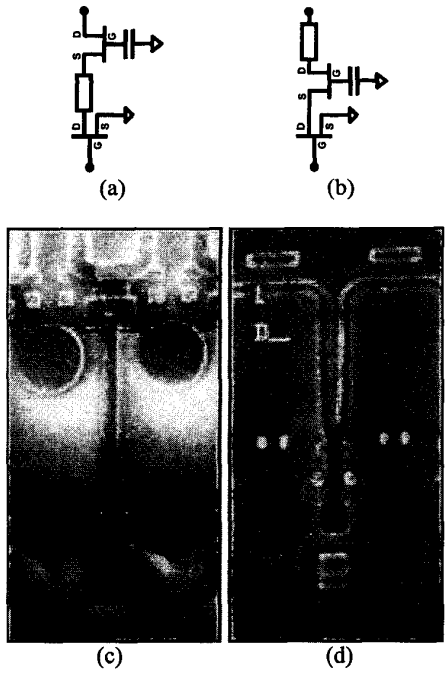

Figure 1. (a,b) Cascode Topologies (c) SEM of the Cascode Cell Implementation (d) Dual Gate Cell

Figure 1c cascode cell's models were fit by using common source (CS) and common gate (CG) FET measurements for the desired cell size and bias. Supporting gate and drain manifolds, vias, and bypassing capacitance along with a standard microstrip transmission line model connecting the two were added to construct the

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entire cascode cell. The dual gate in Figure 1d was fit by using the same intrinsic model starting values which were then optimized to fit measurements of previously manufactured 0.25-μm dual gate cells.

The FET periphery required to achieve greater than 6.5-V_{PP} was based on the I_{MAX} of the active devices and the gain needed for the amplifiers. Capacitive gate division de-couples the gain and output power and permits a periphery large enough to drive high voltages without severely limiting bandwidth [5]. Essentially, it allows the bandwidth limiting to be balanced between the cascode cell's input and output in order to maximize the bandwidth of the entire circuit.

Both amplifiers were designed using eleven cascode cells. They were fabricated on the same wafers with the designation of EG1842-A for the cascode cell implementation and EG1842-D for the dual gate version. The EG1842-A uses 75μm cells for a total periphery of 0.825mm. The EG1842-D used 65μm dual gate cells for a total periphery of 0.715mm. The "A" version's periphery was chosen to be 15% larger than the "D" in order to obtain higher output voltage drive margin in these first pass designs.

The inductive input and output lines were optimized to achieve the desired amount of bandwidth and return losses. The ICs are DC coupled at both the RF input and output and can operate to as low a frequency as allowed by the off-chip bypassing. Wide-band diode power detectors are integrated by resistive coupling to the RF output so that the power levels can be monitored during use in the system. Photographs of the fabricated ICs are shown in Figure 2 and 3.

IV. Measured Results

Both ICs were characterized under CW conditions by fixturing them to carrier plates with bondwires on the input and output RF Pads. The gate and drain termination's bypassing are augmented with 1nF single layer and 100nF end metalized off-chip shunt capacitors. This allows both amplifiers to operate down to low kHz frequencies. Drain bias can be supplied through the RF output with a commercially available bias tees or more conveniently through the on-chip drain termination resistor at the expense of higher die operating voltage and power dissipation. The CS gate is biased through the gate termination resistor with a negative supply to set the drain current of the amplifier and to perform crossing eye adjustment. The CG gate is controlled from a pad and requires a positive voltage that can be varied from 0 to 3.0V for the gain control function. All fixtured measurements shown are for biasing both gate and drain through the on-chip termination resistors. The CG bias

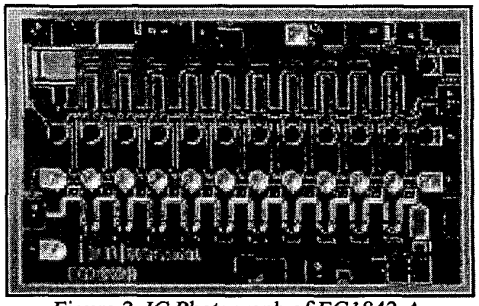

Figure 2. IC Photograph of EG1842-A
1.971 x 1.250 mm (2.464 mm^2)

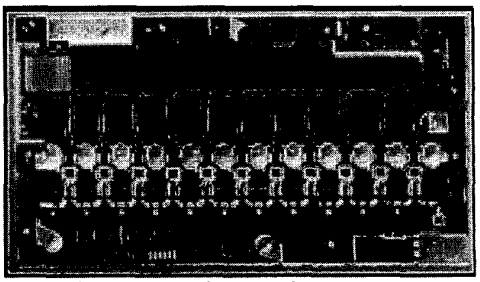

Figure 3. IC Photograph EG1842-D
1.971 x 1.14 mm (2.247 mm^2)

was set at the respective design voltages which was 2.6V for the "A" and 2.0V for the "D".

The "A" and "D" drain quiescent points are 15.7V, 124mA and 13.5V, 108mA for a total DC power dissipation of 1.95 and 1.46W respectively when biased through the termination resistors. S-Parameter measurements are averaged 9 total die randomly chosen from each of the fabricated 3 wafers. In-fixture S-parameter data for the EG1842-A shown in Figure 4 exhibits 42.5GHz 3dB bandwidth. The input and output return losses are better than 12dB through 30GHz. Figure 5 shows the 3dB bandwidth of the EG1842-D is beyond 50GHz and the input and output return losses are better than 12dB through 27GHz. Both Figure 4 and 5 also display the production S-Parameter RF probe one-sigma variation superimposed on the fixtured data. The RF probe sigma is calculated from 900 circuits from the same three wafers. The ± sigma gain variation is 0.53 and 0.78dB for the –A and –D designs respectively at 40GHz. Low sigma indicates a mature fabrication process and the ability to have a high yield for these circuits in production.

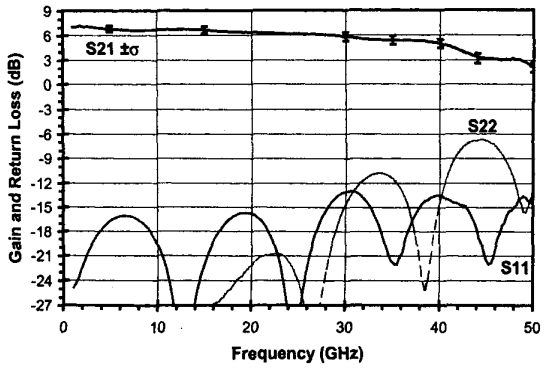

Figure 4. Fixtured EG1842-A S-Parameters

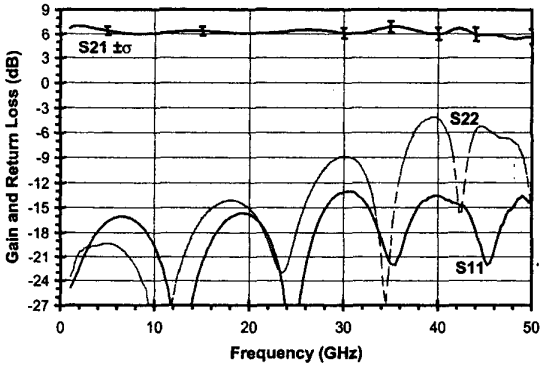

Figure 5. Fixtured EG1842-D S-Parameters

Both amplifier's smooth gain response inherently produce favorable group delay performance. Figure 6 displays the "A" and "D" group delay for the averaged S-Parameters. The "A" has an average group delay of 55ps and is ±5ps up to 37GHz. The "D" has an average group delay of 56ps and is ±5ps up to 32GHz.

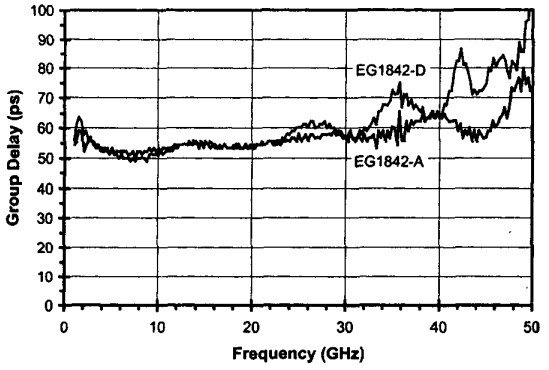

Figure 6. Fixtured Group Delay

Measured in-fixture swept power data for the EG1842-D amplifier is shown in Figure 7 showing that the output power is flat across frequency and is linear up to about 20dBm output power. Figure 8 shows the P1dB for both amplifiers exhibiting better than 22dBm of output power up to 25GHz. The "A" version has about 0.5dB more output power drive capability at lower frequencies due to its larger periphery. Both versions' P1dB output power curves exhibit a frequency slope similar to their gain up to the measured frequencies of 25GHz.

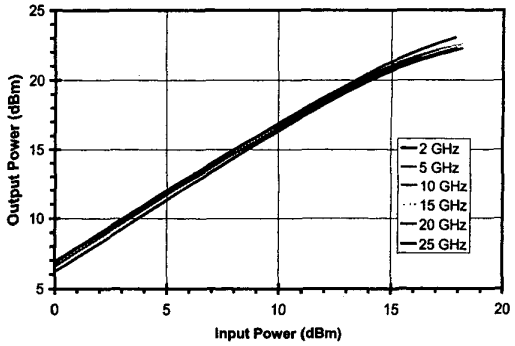

Figure 7. Fixtured EG1842-D Swept Power

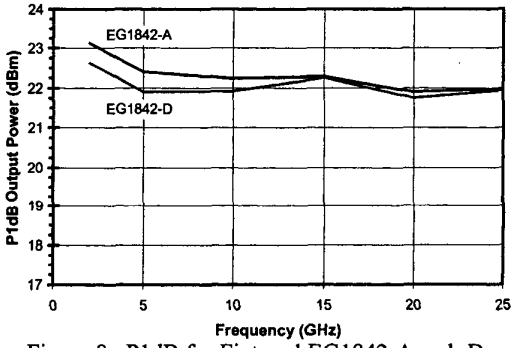

Figure 8. P1dB for Fixtured EG1842-A and -D

Test results for the EG1842–D's 40 Gb/s 2^{31}-1 PRBS data eye diagram are shown in Figure 9. The waveform exhibits a 7.4-V_{PP} swing with a mean high to low value of 5.9V. The losses from the fixtured part's output TFN, microstrip to coax launcher, and coax cable to the test equipment are included in the eye diagram measurements and typically represent 0.5dB loss at 20GHz. Taking this into account, the output power in Figure 8 and the data eye in Figure 9 are consistent with each other. It is expected that both the jitter and mean voltage swing will be improved after circuit tweaks are implemented in subsequent lots.

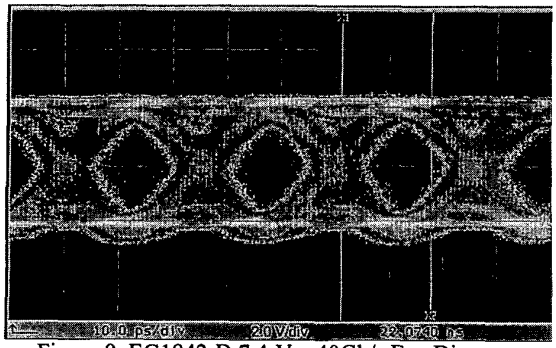

Figure 9. EG1842-D 7.4-V_{PP} 40Gb/s Eye Diagram

Measured results show that the "A" has higher output voltage drive capability at the expense of bandwidth and slightly higher power consumption. Data eyes at 40 Gb/s have not been taken but the "A" 10 Gb/s data eyes have demonstrated that the "A" version can drive 0.8V_{PP} higher voltage due to its larger periphery. The "D" uses a more risky cascode cell implementation that allowed for a 9% reduction in size. The dual gate cell may have contributed to the larger bandwidth than the "A" circuit but this is inconclusive because the two amplifiers have different periphery sizes.

IV. CONCLUSIONS

The design and performance of two high voltage 40Gb/s Fiber Optic E/O Modulator Driver ICs have been presented. The DC-coupled amplifiers use a mature 0.25-μm GaAs pHEMT production process. Measured results demonstrate 6dB small signal gain, larger than 42.5GHz 3dB-bandwidth, and higher than 6.5-V_{PP} output voltage. Both amplifiers have been designed using the least amount of die area possible and have integrated power detectors and level/crossing control, which reduce total circuit and functionality cost. These results demonstrate that a production 0.25-μm pHEMT process can support development of cost competitive 40Gb/s systems.

ACKNOWLEDGEMENTS

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